Claims

What is claimed is:

1. A analog electronic device comprising:

four terminals and means such that

said terminal 1 accepts a current of predetermined direction;
said terminal 2 is receptive to an input signal;
said terminal 3 causes a current to flow;
said terminal 4 has means to concurrently produce an output voltage and current in response to the voltage and current at said terminal 2 and to sense said voltage and current at said terminal 4 and to adjust said voltage and current at said terminal 2 and said current at said terminal 3; and

whereby said device can be used to create amplifiers, cascoding devices, buffers, regulators, and digital circuits with new topologies.

2. A four terminal analog electronic device comprising:

two bipolar transistors of like type or conductivity;

said terminal 1 is the connection of the base of said second transistor and the collector of said first transistor;
said terminal 2 is the emitter of said first transistor;
said terminal 3 is the collector of said second transistor;
said terminal 4 is the connection of the base of said first transistor and the emitter of said second transistor, and;

thereby
said terminal 1 accepts a current of predetermined direction;
said terminal 2 is receptive to an input signal;
said terminal 3 causes a current to flow in a predetermined direction;
said terminal 4 concurrently produces an output voltage and current in response to the voltage and current at said terminal 2 and senses said voltage and current at said terminal 4 and to adjusts said voltage and current at said terminal 2 and said current at said terminal 3; and

whereby said device can be used to create amplifiers, cascoding devices, buffers, regulators, and digital circuits with new topologies.

3. A four terminal analog electronic device comprising:

a bipolar transistor and a FET transistor of like type or conductivity;

said terminal 1 is the connection of the gate of said FET transistor and the collector of said bipolar transistor;
said terminal 2 is the emitter of said bipolar transistor;
said terminal 3 is the drain of said FET transistor;
said terminal 4 is the connection of the base of said bipolar transistor and the source of said FET transistor, and;

thereby
said terminal 1 accepts a current of predetermined direction;
said terminal 2 is receptive to an input signal;
said terminal 3 causes a current to flow in a predetermined direction;
said terminal 4 concurrently produces an output voltage and current in response to the voltage and current at said terminal 2 and senses said voltage and current at said terminal 4 and to adjusts said voltage and current at said terminal 2 and said current at said terminal 3; and

whereby said device can be used to create amplifiers, cascoding devices, buffers, regulators, and digital circuits with new topologies.

4. The device as set forth in claim 1 used as a cascoding device wherein:

said terminal 1 is supplied with a predetermined current,
said terminal 2 is referenced by a predetermined voltage,
said terminal 3 causes a current to flow from a predetermined supply voltage by way of a sensing device, where said sensing device would include, but not limited to, a resistor, base-emitter junction, and current mirror and,
said terminal 4 supplies an object gain transistor with a voltage that is substantially unchanging and any current drawn by said gain transistor is substantially the same as that caused to be drawn by said terminal 3;

whereby as the current drawn by said terminal 3 is substantially the same as the current drawn from said terminal 4 by said gain transistor, said current drawn by said terminal 3 can be used in a similar manner to that of a prior art cascode circuit i.e., to produce a voltage across an impedance, to drive a transistor or to drive a current mirror.

5. The device as set forth in claim 4 wherein:

said gain transistor is a more complicated circuit such as an operational amplifier;

whereby a low voltage integrated operational amplifier can be use with a higher supply voltages and is buffered from those higher voltages by the use a plurality of cascode circuits as taught in claim 4.

6. The device as set forth in claim 1 used to create an amplifier stage wherein:

said device is used to buffer a first current gain stage and drive a second current gain stage;

said terminal 1 is supplied with a predetermined current,
said terminal 2 is referenced by a voltage,
said terminal 3 is supplied with a predetermined supply voltage by way of the base-emitter junction of said second current gain stage and causes a varying current to flow equal to that drawn by said first current gain stage transistor through said base-emitter junction of said second current gain stage,
said terminal 4 supplies said first object gain transistor with a voltage that is substantially unchanging ,
collector of said first current gain stage is connected to a supply voltage of opposite polarity to that supplying terminals 2 and 3 which could be ground, and
collector of said second gain stage is the output of the circuit;

whereby the input current to said first current gain stage produces a current from said second current gain stage equal to beta of said first current gain stage times beta of said second current gain stage times said input current and said output current can drive a load impedance to produce a voltage.

7. The amplifier stage as set forth in claim 6 used to create an amplifier wherein:

two symmetrical stages of claim 6 of opposing polarity are combined;

where said inputs are connected together forming a composite input,
said outputs are connected together forming a composite output and,
said second terminals of said respective symmetrical stages are connected and act as a reference point for the circuit;

whereby a current of either polarity input into said composite input produces a current at said composite output equals to minus beta of said first current gain stage times beta of said second current gain stage where current is amplified by one of said symmetrical stages depending of the polarity of the input current, and;
whereby the amplifier can be used with negative feedback due to the lack of significant offset voltage.

8. The amplifier of claim 7 wherein said reference point is connected to ground.

9. The amplifier of claim 7 wherein said reference point is used functionally as a non-inverting input;

whereby said non-inverting input signal causes amplifier to operate differently depending on impedance of signal;

whereby a current supplied to said non-inverting input produces a current at the output equal to beta of said second transistor times beta of said second current gain stage times input current difference;

whereby if said inputs are driven by voltages instead of currents then output current will be a function of the difference of input voltages.

10. The amplifier of claim 7 comprising:

four (4) NPN transistors, four (4) PNP transistors and two (2) current sources connected as follows:

the base of first PNP transistor is connected to the base of first NPN transistor and is the input of the amplifier;
the collectors of said first NPN and said first PNP transistors are connected to predetermined supply voltages which could include ground;
the emitter of said first PNP transistor is connected to the base of second NPN transistor and to the emitter of third NPN transistor;
the emitter of said first NPN transistor is connected to the base of second PNP transistor and to the emitter of third PNP transistor;
the base of said third NPN transistor is connected to the collector of said second NPN transistor and to one end of a first current source;
the base of said third PNP transistor is connected to the collector of said second PNP transistor and to one end of a second current source;
the emitters of said second NPN and said second PNP transistor are connected together and driven by a signal;
the collector of said third NPN transistor is connected to the base of fourth PNP transistor;
the collector of said third PNP transistor is connected to the base of fourth NPN transistor;
the emitters of said fourth NPN and said fourth PNP transistors are connected to predetermined supply voltages and;
the collectors of said fourth NPN transistor and said fourth PNP transistors are connected together and constitute the output of the invention;

whereby a current of either polarity input into said composite input produces a current at said composite output equals to minus beta of said first current gain stage times beta of said second current gain stage times the input current where the input current is amplified by one of said symmetrical stages depending of the polarity of the input current;

whereby if said input is driven by voltage instead of current then output current will be a function of the difference of said input voltage and said signal voltage at the connection of emitters of said second NPN transistor and said second PNP transistor.

11. The device as set forth in claim 1 used to create a buffer amplifier.

12 The buffer amplifier of claim 11 comprising:

two (2) devices of claim 1 of opposite polarity along with two bipolar transistors and two current sources wherein:

said terminal 2 of each said device is connected to the terminal 2 of other said device and said connection is functionally the input of said buffer;
said terminal 1 of each said device is connected via a current source to a predetermined supply voltage of the correct polarity;
said terminal 3 of each said device is connected to a predetermined supply voltage of the correct polarity;
said terminal 4 of each said device is connected to the base of one of said bipolar transistors of same polarity as that of said device respectively;
collectors of each said bipolar transistor are connected to a predetermined supply voltage of the proper polarity and the emitters of each of said bipolar transistors are connected together and constitutes the output of said buffer amplifier;

whereby an input of a voltage at a low impedance will a substantially equal output voltage, differing only by a varying offset due to the differences of base-emitter voltages of said transistors under varying conditions and;

whereby an input of a current at a high impedance will produce an output current equal to β^2 times said input current.

13. The buffer amplifier of claim 11 comprising:

three (3) PNP transistors, three (3) NPN transistors and two (2) current sources;

the emitters of first NPN transistor and first PNP transistor are connected together and constitute the input;
the collector of said first NPN transistor is connected to the base of the second NPN transistor and to one end of a first current source where opposite end is connected to a predetermined positive supply voltage;

the base of said first NPN transistor is connected to the emitter of said second NPN transistor and the base of third NPN transistor;
the collectors of said second NPN transistor and said third NPN transistor are connected to a predetermined positive supply voltage;
the collector of said first PNP transistor is connected to the base of the second PNP transistor and to one end of a second current source where opposite end is connected to a predetermined negative supply voltage;
the base of said first PNP transistor is connected to the emitter of said second PNP transistor and the base of third PNP transistor;
the collectors of said second PNP transistor and said third PNP transistor are connected to a predetermined positive supply voltage;
the emitters of said third NPN transistor and said third PNP transistor are connected together and constitute the output;

whereby an input of a voltage at a low impedance will produce a substantially equal output voltage, differing only by a varying offset due to the differences of base-emitter voltages of said transistors under varying conditions and;
whereby an input of a current at a high impedance will produce an output current equal to β^2 times said input current only limited by the drive current of the current sources.

14. The buffer amplifier of claim 11 comprising:

two (2) PNP transistors, two (2) NPN transistors, one (1) n-channel MOSFET, one (1) p-channel MOSFET and two (2) current sources;

the emitters of first NPN transistor and first PNP transistor are connected together and constitute the input;
the collector of said first NPN transistor is connected to the gate of the first n-channel MOSFET transistor and to one end of a first current source where opposite end is connected to a predetermined positive supply voltage;
the base of said first NPN transistor is connected to the source of said first n-channel MOSFET transistor and the base of second NPN transistor;
the drain of said first n-channel MOSFET transistor and the collector of said second NPN transistor are connected to a predetermined positive supply voltage;
the collector of said first PNP transistor is connected to the base of the first p-channel MOSFET transistor and to one end of a current source where opposite end is connected to a predetermined negative supply voltage;
the base of said first PNP transistor is connected to the source of said first p-channel MOSFET transistor and the base of second PNP transistor;
the drain of said first p-channel MOSFET transistor and the collector of said second PNP transistor are connected to a predetermined positive supply voltage;
the emitters of said second NPN transistor and said second PNP transistor are connected together and constitute the output;

whereby an input of a voltage at a low impedance will produce a substantially equal output voltage, differing only by a varying offset due to the differences of base-emitter voltages of said transistors under varying conditions and;
whereby an input of a current at a high impedance will produce an output current greater than that seen using bipolar transistors in place of the MOSFET transistors.

15. The device as set forth in claim 1 used to create a voltage regulator.

16. The device as set forth in claim 1 used to create a digital circuit

wherein said digital circuit can include OR gates and NOR gates.

17. The OR gate digital circuit as set forth in claim 16 comprising:

three (3) NPN transistors, one (1) PNP transistors and two (2) current sources connected as follows:

the collector of a first NPN transistor and the base of a second NPN transistor are connected to the emitter of a third NPN transistor;
the collector of said second NPN transistor and the base of said third NPN transistor are connected to one end of a first current course where opposite end of said first current source is connected to a predetermined positive supply voltage;
the emitters of said first NPN transistor and said second NPN transistor are connected to a reference voltage which includes ground;
the collector of said third NPN transistor is connected to the base of a first PNP transistor;
the emitter of said first PNP transistor is connected to a predetermined positive supply voltage;
the collector of said first PNP transistor is connected to one end of a second current source where the opposite end of said second current source is connected to said reference voltage and this connection constitutes the output of the circuit; and
the base of said first NPN transistor is the input of the circuit;

whereby the absence of an input signal causes the output to go to a low voltage;

whereby an input signal below 500 mV causes the output to go to a low voltage;

whereby the presence of a high input signal causes the output to saturate to the positive supply voltage with a current capability of beta of said third NPN transistor times beta of said first PNP transistor times the current supplied by said first current source;

whereby the ratio of output current to required input current is basically equal to the beta of said first NPN transistor times the beta of said first PNP transistor where such figure called fan-out is on the order of 10,000;

whereby said digital circuit can operate on a voltage below 1.5 volts.

18. The NOR gate digital circuit as set forth in claim 16 comprising:

two (2) NPN transistors, two (2) PNP transistors, one (1) diode and three (3) current sources connected as follows:

the base of a first PNP transistor is connected to one end of a first current source and this connection is the input of the digital circuit, where opposite end of said first current source is connected to a reference voltage which can include ground;
the collector of said first PNP transistor is connected to said reference voltage;
the emitter of said first PNP transistor is connected to the base of first NPN transistor and to the emitter of second NPN transistor;
the emitter of said first NPN transistor is connected to a diode where opposite end of diode is connected to said reference voltage;
the base of said second NPN transistor is connected to the collector of said first NPN transistor and to one end of a second current source, where said second current source is connected to a predetermined positive supply voltage;
the base of said second PNP transistor is connected to the collector of said second NPN transistor;
the emitter of said second PNP transistors is connected to a predetermined positive supply voltages and;
the collector of said second PNP transistors is connected to is the output of the device and is further connected to a third current source where opposite end of said third current source is connected to said reference voltage;

whereby the absence of an input signal causes the output to saturate to the positive supply voltage with a current capability of beta of said first PNP transistor times beta of said second PNP transistor times the current drawn by said first current source;

whereby the presence of a high input signal the output goes into a off state where there is some current being output which can swamped by the said third current source as such output current is of the order of the current being supplied by said second current source;

whereby the ratio of output current to required input current is basically equal to the beat of said first PNP transistor times the beta of said second PNP transistor and such figure called fan-out is on the order of 10,000;

whereby said digital circuit can operate on a voltage below 2 volts.

19. The NOR gate digital circuit as set forth in claim 16 comprising:

two (2) NPN transistors, three (3) PNP transistors and three (3) current sources connected as follows:

the base of a first PNP transistor and the base of a second PNP transistor are connected to one end of a first current source and this connection is the input of the digital circuit, where opposite end of said current source is connected to a reference voltage which can include ground;
the collectors of said first PNP transistor and said second PNP transistors are connected to said reference voltage;
the emitters of said first PNP transistor and said second PNP transistor are connected to the base of first NPN transistor and to the emitter of second NPN transistor;
the emitter of said first NPN transistor is connected to said reference voltage;
the base of said second NPN transistor is connected to the collector of said first NPN transistor and to one end of a second current source, where said second current source is connected to a predetermined positive supply voltage;
the base of said third PNP transistor is connected to the collector of said second NPN transistor;
the emitter of said third PNP transistors is connected to a predetermined positive supply voltages and;
the collector of said third PNP transistors is connected to is the output of the device and is further connected to a third current source where opposite end of said third current source is connected to said reference voltage;

whereby the absence of an input signal causes the output to saturate to the positive supply voltage with a current capability of beta of said first PNP transistor times beta of said third PNP transistor times the current drawn by said first current source;

whereby the presence of a high input signal the output goes into a off state where there is some current being output which can swamped by the said third current source as such output current is of the order of the current being supplied by said second current source;

whereby the ratio of output current to required input current is basically equal to the beta of said first PNP transistor times the beta of said third PNP transistor and such figure called fan-out is on the order of 10,000;

whereby said digital circuit can operate on a voltage below 1.5 volts.

20. The device as detailed in Claims 1 wherein said means comprising:

two bipolar transistors of like type or conductivity;

said terminal 1 is the connection of the base of said second transistor and the collector of said first transistor;
said terminal 2 is the emitter of said first transistor;
said terminal 3 is the collector of said second transistor;
said terminal 4 is the connection of the base of said first transistor and the emitter of said second transistor, and;

thereby
said terminal 1 accepts a current of predetermined direction;
said terminal 2 is receptive to an input signal;
said terminal 3 causes a current to flow in a predetermined direction;
said terminal 4 concurrently produces an output voltage and current in response to the voltage and current at said terminal 2 and senses said voltage and current at said terminal 4 and to adjusts said voltage and current at said terminal 2 and said current at said terminal 3; and

whereby said device can be used to create amplifiers, cascoding devices, buffers, regulators, and digital circuits with new topologies.

21. The device as detailed in Claims 1 wherein said means comprising:

a bipolar transistor and a FET transistor of like type or conductivity;

said terminal 1 is the connection of the gate of said FET transistor and the collector of said bipolar transistor;
said terminal 2 is the emitter of said bipolar transistor;
said terminal 3 is the drain of said FET transistor;
said terminal 4 is the connection of the base of said bipolar transistor and the source of said FET transistor, and;

thereby
said terminal 1 accepts a current of predetermined direction;
said terminal 2 is receptive to an input signal;
said terminal 3 causes a current to flow in a predetermined direction;
said terminal 4 concurrently produces an output voltage and current in response to the voltage and current at said terminal 2 and senses said voltage and current at said terminal 4 and to adjusts said voltage and current at said terminal 2 and said current at said terminal 3; and

whereby said device can be used to create amplifiers, cascoding devices, buffers, regulators, and digital circuits with new topologies.